REMARKS

Claims 1 to 22 and 30 to 39 remain active in this application without amendment.

Claims 30 to 39 were rejected under 35 U.S.C. 102(e) as being anticipated by Kalidas et al. (U.S. 6,396,136). The rejection is respectfully traversed for several reasons.

To begin with, the fact that Kalidas et al. has a provisional application filing date prior to the provisional application filing date of the subject application does not automatically carry the filing date of Kalidas et al. back to the filing date of the provisional application. There is a further requirement that the subject matter in the cited Kalidas et al. patent alleged to anticipate the rejected claims also be found in the provisional application. This has not been shown on the record and, accordingly, the Kalidas et al. patent is not a proper reference on the present record for this reason alone.

In addition, Kalidas et al. was copending with the subject application and is assigned to the same assignee as the subject application. Accordingly, Kalidas et al. is not available as a reference in this application for that reason as well in view of 35 U.S.C. 103(c).

Kalidas et al. fails to anticipate any of the rejected claims. With reference to claim 30, this claim requires, among other features, a substrate having first and second opposing surfaces and having thereon both an integrated circuit and a plurality of signal lines, a plurality of first power lines coupleable to a first power source, and a plurality of second power lines coupleable to a second power source, all on the second surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines, and the signal lines between the pair of the plurality of first power lines and the pair of

the plurality of first power lines disposed between a pair of the second power lines. No such combination of features is taught by Kalidas et al.

Claims 31 to 33 depend from claim 30 and therefore are not anticipated by Kalidas et al.

Claim 34 requires a substrate having first and second opposing surfaces and having thereon both an integrated circuit chip and a plurality of groups of lines, the plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in ~~a~~ the second group of lines of the second width are disposed between lines of the third width. No such combination of features is taught by Kalidas et al.

Claims 35 and 36 depend from claim 34 and therefore are not anticipated by Kalidas et al.

Claim 37 requires a substrate having first and second opposing surfaces and having thereon both an integrated circuit chip and a plurality of signal lines, a plurality of first power lines coupled to a first power source, and a plurality of second power lines coupled to a second power source, all on the second surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines, and the signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines disposed between a pair of the second power lines. No such combination of features is taught by Kalidas et al.

Claims 38 and 39 depend from claim 37 and therefore are not anticipated by Kalidas et al.

Still further, in view of the Declaration of the undersigned, the subject application bears a date of invention prior to the provisional application date of Kalidas et al. In this regard, reference is invited to the decision by the United States Supreme Court in Pfaff v Wells Electronics, 525 U.S. 55 (U.S. 1998) wherein the meaning of the term "invention" was specifically defined as it applies to 35 U.S.C.

It is clear from reading 35 U.S.C. that the word "invention" in the statute "does not contain any express requirement that an invention must be reduced to practice" as stated in Pfaff (though the subject invention was also reduced to practice prior to the provisional filing date of Kalidas et al. as demonstrated in the attached Declaration of Jay M. Cantor) and even in section 102(g) where the conception and reduction to practice are specifically mentioned, there is no requirement that these be the only factors considered. If follows, first, that 35 U.S.C. nowhere defines "invention" by a determination solely of the questions of reduction to practice or conception with diligence up to a reduction to practice (actual or constructive). While a proper showing of a reduction to practice or conception with diligence up to a reduction to practice does establish invention under 35 U.S.C, there is nothing in 35 U.S.C. which limits the definition of invention to only those factors. This is confirmed in Pfaff wherein the Court rejected the longstanding precedent set forth above by stating:

> [III] "Pfaff nevertheless argues that longstanding precedent buttressed by the strong interest in providing inventors with a clear standard identifying the onset of the 1-year period, justifies a special interpretation of the word 'invention' as used in § 102(b). We are persuaded that this nontextual argument should be rejected."

As stated in the opinion in defining the term "invention", the Court states that "Thus petitioner's argument calls into question the standard applied by the Court of Appeals, but it does not persuade us that it is necessary to engraft a reduction to practice element into the meaning of the term 'invention' as used in § 102(b)."

The Court further states:

> "The word 'invention' must refer to a concept that is complete, rather than merely one that is 'substantially complete.' It is true that reduction to practice ordinarily provides the best evidence that an invention is complete. But just because reduction to practice is sufficient evidence of completion, it does not follow that proof of reduction to practice is necessary in every case. Indeed, both the facts of the Telephone Cases and the facts of this case demonstrate that one can prove that an invention is complete and ready for patenting before it has actually been reduced to practice."

The Court concluded that the on-sale bar applies when two conditions are satisfied, the first condition not being applicable in this case because it relates to conditions of sale. However, the second condition relates to the definition of "invention" and states:

> "Second, the invention must be ready for patenting. That condition may be satisfied in at least two ways: by proof of reduction to practice before the critical date; or by proof that prior to the critical date the inventor had prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention. In this case the second condition of the on-sale bar is satisfied because the drawing Pfaff sent to the manufacturer before the critical date fully disclosed the invention: (underline not in original)

It follows that there is an invention disclosure is provided which contains "prepared drawing or other descriptions of the invention that were sufficiently specific to enable a person skilled in the art to practice the invention".

If follows that the subject application contains a disclosure which is ready for patenting as defined by the Supreme Court in Pfaff prior to the provisional application filing date of Kalidas et al.

Still further, as evidenced by the Declaration of Jay M. Cantor, the subject disclosure was reduced to practice prior to the filing date of Kalidas et al.

Claim 34 was rejected under 35 U.S.C. 102(e) as being anticipated by Washida et al. (U.S. 5,877,548) The rejection is respectfully traversed.

Claim 34 requires, among other features, a substrate having first and second opposing surfaces, said substrate having thereon and a plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in a said second group of lines of said second width are disposed between lines of said third width. No such structure is taught or suggested by Washida et al. The lines of Washida et al. are not shown to be all disposed on the substrate 51, but rather extending from the package 21.

Claim 34 further requires an integrated circuit chip mounted on the substrate and coupled to at least some of the lines. The term "some" requires more than one. No plurality of lines on a substrate is shown coupled to the chip of Washida et al.

Claim 34 was rejected under 35 U.S.C. 102(b) as being anticipated by Link et al. (U.S. 5,055,704). The rejection is respectfully traversed.

Claim 34 requires, among other features, a plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the

substrate, the groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in a said second group of lines of said second width are disposed between lines of said third width. No such structure is taught or suggested by Link et al. Clearly, Link et al. does not have groups of lines of the same width, let alone three such groups. The widths of the lines of Link et al. are nowhere stated and appear to be random.

Claim 34 further requires that there be a substrate having first and second opposing surfaces and having thereon an integrated circuit chip and a plurality of groups of lines, the plurality of groups of lines including groups of lines of at least three different widths disposed on the second surface of the substrate, the groups of lines arranged such that one or more lines in a first group of lines of a first width are disposed between lines of a second group of lines of a second width and lines in ~~a~~ the second group of lines of the second width are disposed between lines of the third width. No such combination is taught or suggested by Link et al. Note that the chip 132 of Link et al. is not disposed on the same substrate as the lines. It follows that Link et al. fails to anticipate claim 34 for this reason as well.

Claims 30 to 39 were rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi (U.S. 5,497,030). The rejection is respectfully traversed.

Claim 30 requires, among other features, a substrate having first and second opposing surfaces, having an integrated circuit chip mounted on the substrate and having a plurality of signal lines, a plurality of first power lines coupleable to a first power source, and a plurality of second power lines coupleable to a second power source, all on the second surface, at least one of the plurality of signal lines disposed between a pair of the plurality of first power lines, and the signal lines between the pair of the plurality of first power lines

and the pair of the plurality of first power lines disposed between a pair of the second power lines. No such combination is taught or suggested by Takeuchi. To begin with, the lines of Takeuchi and the chip of Takeuchi are not mounted on the same substrate as required by claim 30. In addition, specific arrangement of the lines is not taught or suggested by Takeuchi. as stated in the Summary of Invention, a high-performance, high input/output ball grid array substrate is provided, which is designed for integrated circuit flip-chip assembly and has two patterned metal layers and an intermediate insulating layer. The insulating layer has a plurality of vias filled with metal, and one of the metal layers attached to each surface. Positioned between the two metal layers, the insulating layer has a thickness and material characteristics suitable for strong electromagnetic coupling between the signal lines and the first metal layer. In this manner, a predetermined impedance to ground is provided, and cross-talk between signal lines is minimized. It is an aspect of the invention that the signal lines are distributed relative to the first power lines such that the inductive coupling between them reaches at least a minimum value, providing high mutual inductances and close to zero effective self-inductance. Further, the signal lines are electromagnetically coupled to the ground metal such that cross-talk between signal lines is minimized. This distribution is provided by arrangement of the signal lines in the manner claimed. No such concept is taught or even remotely suggested by Takeuchi.

Claims 31 to 33 depend from claim 30 and therefore define patentably over Takeuchi for at least the reasons presented above with reference to claim 30.

In addition, claim 31 further limits claim 30 by requiring that the signal lines be of a first width, the first power lines be of a second width different from the first, and the

Claim 39 further limits claim 38 by requiring that the third width be wider than the second width and the second width is wider than the first width. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.

In view second power lines be of a third width different from the first and second widths. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.

Claim 32 further limits claim 31 by requiring that the third width be wider than the second width and the second width be wider than the first width. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.

Claim 33 further limits claim 30 by requiring a ground plane on the first surface of the substrate. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.

Claims 34 and 37 set forth substantially at least the same features discussed above with reference to claims 30 and, accordingly, the arguments presented above with reference to claim 30 apply as well to claim 34.

Claims 35 and 36 depend from claim 34 and claims 38 and 39 depend from claim 37 and therefore define patentably over Takeuchi for at least the reasons presented above with reference to claim 34.

In addition, claim 35 further limits claims 34 and 37 by requiring that the lines of the first width be signal lines, the lines of the second width be power lines coupled to a first voltage potential, and the lines of the third width be power lines coupled to a second voltage potential. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.

Claim 36 further limits claim 34 by requiring a ground plane on the first surface of the substrate. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.

Claim 38 further limits claim 37 by requiring that the signal lines be of a first width, the first power lines be of a second width different from the first, and the second power lines be of a third width different from the first and second widths. No such feature is taught or suggested by Takeuchi either alone or in the combination as claimed.of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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